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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,063	10/15/2001	Jin-Hsin Yang	ASU 128	1643

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EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,063	YANG, JIN-HSIN	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1and 3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The sections relied upon by the Applicant as support for the claim amendments do not support the claim amendments. The first section, page 2, line 8, is used to describe the prior art and states "(warning) signal is sent to the computer system". The second section page 12, lines 7 and 12, simply states "It is capable of detecting all possible error data" and "(data) corruption by detecting al possible FDC defection in (advance)." None of these sections support "determining for all of the data transferred to the floppy diskette, if a requested computer system operation accesses the data from the floppy diskette controller".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fritz et al., US 2002/0016850 A1, and further in view of Adams, U.S. Patent 5,983,002.

Referring to claim 1:

a. In paragraph 0012, Fritz et al. disclose a data communication system (a computer system having a central processing unit). Further, in paragraph 0031, Fritz et al. disclose a system interrupt clock.

b. In paragraph 0033, Fritz et al. disclose that the underrun prevention unit controls the delay between the start of a write access to the buffer's write port and the start of a read access via the buffer's read port (providing a direct memory access (DMA) request (DREQ) and a DMA acknowledgement (DACK), the DREQ being issued when data transfer is requested by the computer system and the DACK being issued when data transfer is permitted).

c. In paragraph 0014, Fritz et al. disclose that the invention can be implemented in processors or other devices having a variable clock rate or transmission rate. However, Fritz et al. don't explicitly disclose a floppy diskette, a floppy diskette controller for controlling the data transfer to the floppy diskette, and peripherals associated with the floppy diskette controller for providing a direct memory access (DMA). In column 7, lines 6-12, Adams discloses that the media driver may be responsible for sending instructions and control signals to the media drive controller which is typically embodied as a floppy diskette controller. Similarly, the media driver may instruct and control the DMA controller. The DMA controller manages data transfers between the floppy

diskette controller and the main memory device. Further, in column 7, lines 12-17, Adams discloses that a DMA request (DREQ) may pass from FDC controller to the direct memory access controller. Likewise, a DMA acknowledge (DACK) may be returned from the DMA controller to the FDC. It would have been obvious to one of ordinary skill at the time of the invention to include the floppy diskette and floppy diskette controller of Adams into the system of Fritz et al. A person of ordinary skill in the art would have been motivated to make the modification because as stated above, Fritz et al. state that the invention can be implemented in processors or other devices having a variable clock rate or transmission rate. This is typical to floppy diskettes and their controllers as evidenced by Adams in column 1, lines 36-48, where Adams discloses in the Background that when the data transferred is to and from a Floppy Diskette Controller ("FDC"), the FDC is responsible for interfacing the computer's Central Processing Unit ("CPU") with the physical diskette drive. Significantly, since the diskette is spinning, it is necessary fro the FDC to provide data to the diskette drive at a specified data rate. Otherwise, the data will be written to a wrong location on the diskette. Therefore, it is necessary to provide a specific data rate in the system of Adams with the invention of Fritz et al. Both patent references are concerned with solving the same problem.

d. Determining for all of the data transferred to the floppy diskette, if a requested computer system operation accesses the data from the floppy diskette controller is inherent to the combined system of Fritz et al. and Adams.

e. In paragraph 0034, Fritz et al. disclose that the length of a time gap between the completion of writing data into the buffer and completion of reading data from the buffer is determined (measuring the time for the DMA request (DREQ) from the issue to the removal thereof).

f. In paragraph 0034, Fritz et al. disclose that the length of a predetermined delay time is decreased by a first value and the length of the predetermined delay time is increased by a second value if the length of the time gap is smaller than the specified tolerance value. Further, in column 1, lines 46-49, Adams discloses that whenever this situation occurs, the FDC aborts the write operation and signals to the CPU that a data underrun condition has occurred (signaling an error from the computer system if the measured time exceeds a specific value).

Referring to claim 2:

a. In paragraph 0033, Fritz et al. dislcose that the underrun prevention unit controls the delay between the start of a write access to the buffer's write port and the start of a read access via the buffer's read port (pre-hooking an interpose service routine to an interrupt vector intercepted by the system interrupt clock).

b. In paragraph 0034, Fritz et al. disclose that the length of a predetermined delay time is decreased by a first value and the length of the predetermined delay time is increased by a second value if the length of the time gap is smaller than the specified tolerance value (increasing an interrupt rate provided by the system interrupt clock, wherein said measuring time is performed through the interpose service routine for every interrupt; and recovering the system interrupt

clock to interrupt normally after the floppy diskette data transfer is completed and unhooking the interrupt vector).

Referring to claim 3:

a. In paragraph 0012, Fritz et al. disclose a data communication system (a computer system having a central processing unit). Further, in paragraph 0031, Fritz et al. disclose a system interrupt clock.

b. In paragraph 0033, Fritz et al. disclose that the underrun prevention unit controls the delay between the start of a write access to the buffer's write port and the start of a read access via the buffer's read port (providing a direct memory access (DMA) request (DREQ) and a DMA acknowledgement (DACK), the DREQ being issued when data transfer is requested by the computer system and the DACK being issued when data transfer is permitted).

c. In paragraph 0014, Fritz et al. disclose that the invention can be implemented in processors or other devices having a variable clock rate or transmission rate. However, Fritz et al. don't explicitly disclose a floppy diskette, a floppy diskette controller for controlling the data transfer to the floppy diskette, and peripherals associated with the floppy diskette controller for providing a direct memory access (DMA). In column 7, lines 6-12, Adams discloses that the media driver may be responsible for sending instructions and control signals to the media drive controller which is typically embodied as a floppy diskette controller. Similarly, the media driver may instruct and control the DMA controller. The DMA controller manages data transfers between the floppy

diskette controller and the main memory device. Further, in column 7, lines 12-17, Adams discloses that a DMA request (DREQ) may pass from FDC controller to the direct memory access controller. Likewise, a DMA acknowledge (DACK) may be returned from the DMA controller to the FDC. It would have been obvious to one of ordinary skill at the time of the invention to include the floppy diskette and floppy diskette controller of Adams into the system of Fritz et al. A person of ordinary skill in the art would have been motivated to make the modification because as stated above, Fritz et al. state that the invention can be implemented in processors or other devices having a variable clock rate or transmission rate. This is typical to floppy diskettes and their controllers as evidenced by Adams in column 1, lines 36-48, where Adams discloses in the Background that when the data transferred is to and from a Floppy Diskette Controller ("FDC"), the FDC is responsible for interfacing the computer's Central Processing Unit ("CPU") with the physical diskette drive. Significantly, since the diskette is spinning, it is necessary fro the FDC to provide data to the diskette drive at a specified data rate. Otherwise, the data will be written to a wrong location on the diskette. Therefore, it is necessary to provide a specific data rate in the system of Adams with the invention of Fritz et al. Both patent references are concerned with solving the same problem.

d. Determining for all of the data transferred to the floppy diskette, if a requested computer system operation accesses the data from the floppy diskette controller is inherent to the combined system of Fritz et al. and Adams.

e. In paragraph 0034, Fritz et al. disclose that the length of a predetermined delay time is decreased by a first value and the length of the predetermined delay time is increased by a second value if the length of the time gap is smaller than the specified tolerance value (programming the system interrupt clock to increase an interrupt rate provided by the system interrupt clock, wherein the existence of the DMA request (DREQ) is detected for every interrupt issued by the system interrupt clock; and reprogramming the system interrupt clock to recover the interrupt at a normal rate).

f. In paragraph 0034, Fritz et al. disclose that the length of a time gap between the completion of writing data into the buffer and completion of reading data from the buffer is determined (measuring the time for the DMA request (DREQ) from the issue to the removal an recording a maximum time).

g. In paragraph 0034, Fritz et al. disclose that the length of a predetermined delay time is decreased by a first value and the length of the predetermined delay time is increased by a second value if the length of the time gap is smaller than the specified tolerance value. Further, in column 1, lines 46-49, Adams discloses that whenever this situation occurs, the FDC aborts the write operation and signals to the CPU that a data underrun condition has occurred (signaling an error from the computer system if the measured time exceeds a specific value).

Response to Arguments

5. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,949,971	Levine et al.
U.S. Patent 6,665,728 B1	Graumann et al.
U.S. Patent 6,751,038 B1	Wada
US 2002/0012297 A1	Suzuki

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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